PRODUCT INFORMATION

ISSUED DATE : 2009-11-30

SAMSUNG TFT-LCD PRODUCT INFORMATION

MODEL : LTM230HU02

Note : This is Product Information is subject to change after 3 months of issuing date.

Application Engineering Part 1, TCS team

LCD Division, Samsung Electronics Co . , LTD.

Contents

PRODUCT INFORMATION

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General Description

Description

LTM230HU01 is a color active matrix liquid crystal display (LCD) that uses amorphous silicon TFT (Thin Film Transistor) as switching components. This model is composed of a TFT LCD panel, a driver circuit and a back light unit. The resolution of a 23" is 1920 x 1080 and this model can display up to 16.7 millions colors.

Features

- High contrast ratio, high aperture structure
- TN (Twisted Nematic) mode
- Wide Viewing Angle
- High speed response
- FHD (1920 x 1080 pixels) resolution
- Low power consumption
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface (4pixel/clock)
- RoHS compliance

Applications

- Workstation & desktop monitors
- Display terminals for AV application products
- Monitors for Entertainment
- Monitors for industrial machine

* If the module is used to other applications besides the above, please contact SEC in advance.

General Information

Items	Specification	Unit	Note
Pixel Pitch	0.2655(H) x 0.2655(W)	mm	
Active Display Area	509.76(H) x 286.74(V)	mm	
Surface Treatment	Reflection Ratio 4%, Glare		
Display Colors	16.7M (Hi-FRC)	colors	
Number of Pixels	1,920 x 1,080	pixel	
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally White		
Luminance of White	300(Typ.)	cd/㎡	

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	533.5	534.0	534.5	mm	w/o inverter ass'y
	Vertical (V)	311.2	311.7	312.2	mm	
	Depth (D)	-	-	19.5	mm	
Weight		-	-	3,000	g	LCD module only

Note (1) Mechanical tolerance is ± 0.5mm unless there is a special comment.

1. Absolute Maximum Ratings

If the condition exceeds maximum ratings, it can cause malfunction or unrecoverable damage to the device.

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	GND-0.5	6.5	V	(1)
Storage temperature	T_{STG}	-25	60	℃	(2)
Center of Glass surface temperature (Operation)	T_{OPR}	0	50	℃	(2)
Shock (non - operating)	S_{nop}	-	50	G	(3)(5)
Vibration (non - operating)	V_{nop}	-	1.5	G	(4)(5)

Note (1) Ta= 25 ± 2 °C

(2) Temperature and relative humidity range are shown in the figure below.
a. 90 % RH Max. (Ta ≤ 39 °C)
b. Maximum wet-bulb temperature at 39 °C or less. (Ta ≤ 39 °C)
c. No condensation
(3) 11ms, sine wave, one time for ±X, ±Y, ±Z axis
(4) 10-300 Hz, Sweep rate 10min, 30min for X,Y,Z axis
(5) At vibration and shock test, the fixture which holds the module to be tested has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

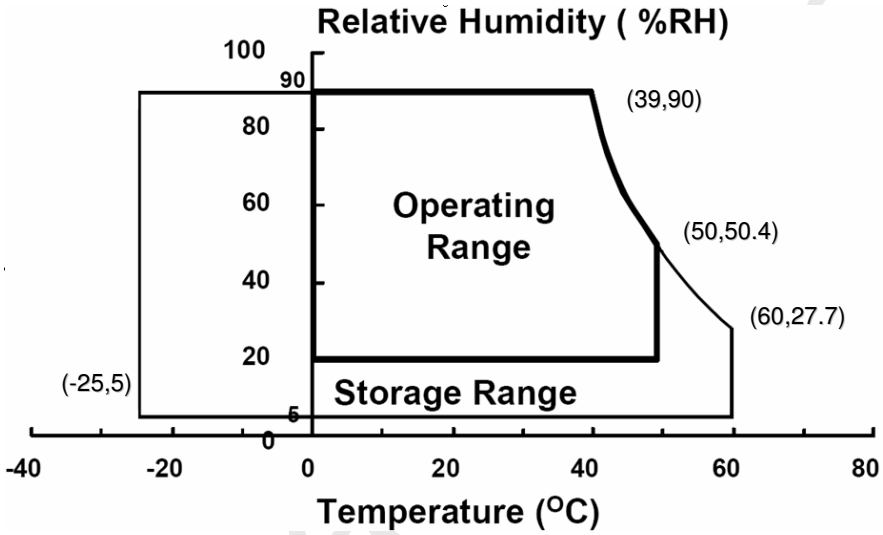


Fig. Temperature and Relative humidity range

2. Optical Characteristics

The optical characteristics should be measured in a dark room or equivalent.
Measuring equipment : SR-3, RD-80S (TOPCON), EZ-Contrast (Eldim)

(Ta = 25 ± 2°C, VDD=5V, fv= 120Hz, fDCLK= 70 MHz, IL = 7.5mArms)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center of screen)		C/R		700	1000	-		(3) SR-3
Response Time(On/Off)	G/G	Tr + Tf		-	3	-	msec	(5) RD-80S
Luminance of White (Center of screen)		Y_L		250	300	-	cd/m^2	(6) SR-3
Color Chromaticity (CIE 1931)	Red	Rx	Normal $\Theta_{L,R}=0$ $\Theta_{U,D}=0$ Viewing Angle	-0.030	0.646	+0.030		(7),(8) SR-3
		Ry			0.333			
	Green	Gx			0.304			
		Gy			0.601			
	Blue	Bx			0.149			
		By			0.058			
	White	Wx			0.313			
		Wy			0.329			
Color Chromaticity (CIE 1976)	Red	Ru'		-	0.453	-		
		Rv'		-	0.528	-		
	Green	Gu'		-	0.122	-		
		Gv'		-	0.563	-		
	Blue	Bu'		-	0.163	-		
		Bv'		-	0.187	-		
	White	Wu'		-	0.198	-		
		Wv'		-	0.468	-		
C.G.L (ACC ONLY)	White	△u'v'		-	-	0.02		(9)

* C.G.L : Color Grayscale Linearity

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Temperature		-		-	6500	-	K	
Color Gamut		-		-	72	-	%	CIE1931
Viewing Angle	Hor.	Θ_L	CR≥10	70	80	-	Degrees	(8) SR-3
		Θ_R		70	80	-		
	Ver.	Θ_U		70	80	-		
		Θ_D		70	80	-		
Brightness Uniformity (9 Points)		B_{uni}		-	-	25	%	(4) SR-3

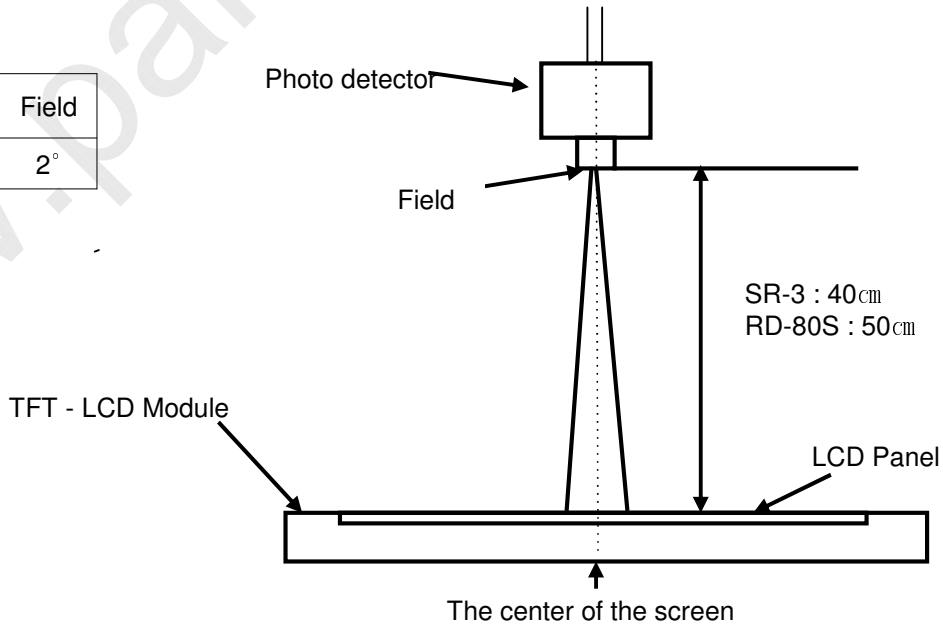
Note (1) Test Equipment Setup

The measurement should be executed in a stable, windless and dark room between 30min after lighting the back light at the given temperature for stabilization of the back light. This should be measured in the center of screen.

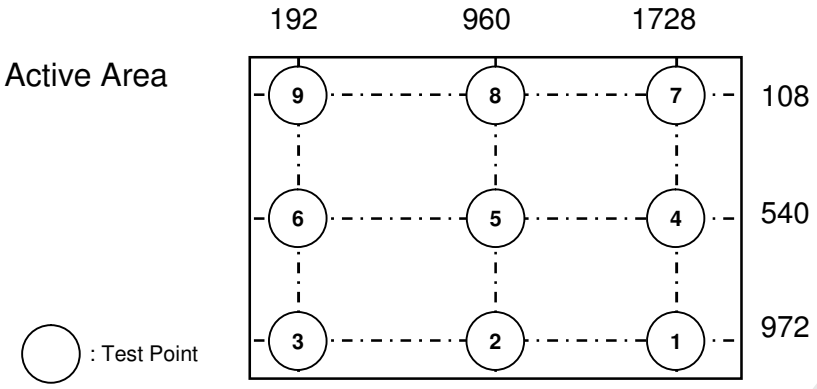
Single lamp current : 7.5mA

Environment condition : Ta = 25 ± 2 °C

Photo detector	Field
SR-3	2°



Note (2) Definition of test point



Note (3) Definition of Contrast Ratio (C/R)
: Ratio of gray max (Gmax) & gray min (Gmin) at the center point⑤ of the panel

$$CR = \frac{G\max}{G\min}$$

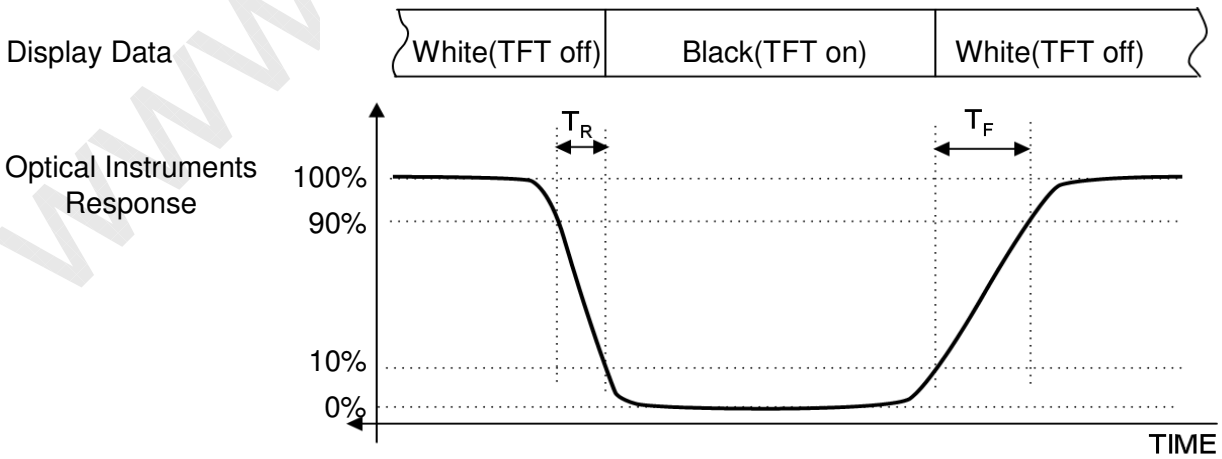
Gmax : Luminance with all pixels white
Gmin : Luminance with all pixels black

Note (4) Definition of 9 points brightness uniformity

$$Buni = 100 \times \frac{(B\max - B\min)}{B\max}$$

Bmax : Maximum brightness
Bmin : Minimum brightness

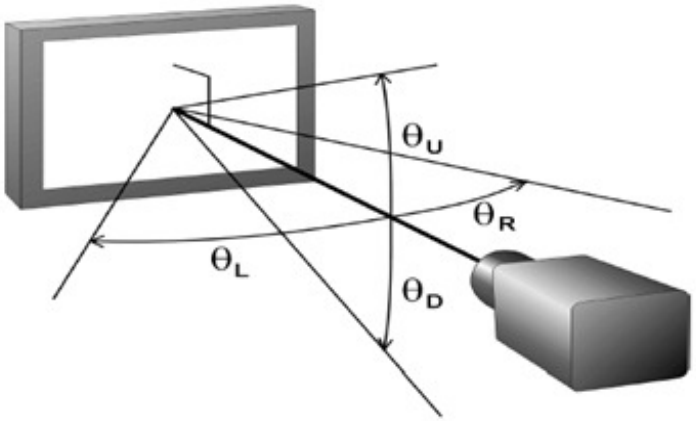
Note (5) Definition of Response time : Sum of Tr, Tf



Note (6) Definition of Luminance of White : Luminance of white at center point⑤

Note (7) Definition of Color Chromaticity (CIE 1931, CIE1976)
Color coordinate of Red, Green, Blue & White at center point⑤

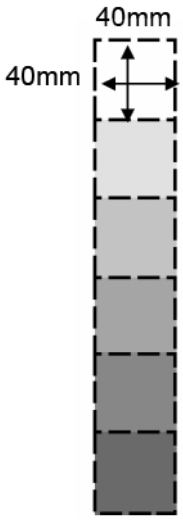
Note (8) Definition of Viewing Angle
: Viewing angle range (CR ≥ 10)



Note (9) Color Grayscale Linearity

a. Test image : 100% full white pattern with a test pattern as below

b. Test pattern : Squares, 40mm by 40mm in size, filled with 255, 225, 195, 165, 135 and 105 grays steps should be arranged at the center⑤ of the screen.



c. Test method

-1st gray step : move a square of 255 gray level should be moved into the center of the screen and measure luminance and u' and v' coordinates.

- Next gray step : Move a 225 gray square into the center and measure both luminance and coordinates, too.

d. Test evaluation

$$\Delta u'v' = \sqrt{(u'_A - u'_B)^2 + (v'_A - v'_B)^2}$$

Where A, B : 2 gray levels found to have the largest color differences between them

i.e. get the largest Δu' and Δv' of each 6 pair of u' and v' and calculate the Δu'v'.

3. Electrical Characteristics

3.1 TFT LCD Module

The connector for display data & timing signal should be connected.

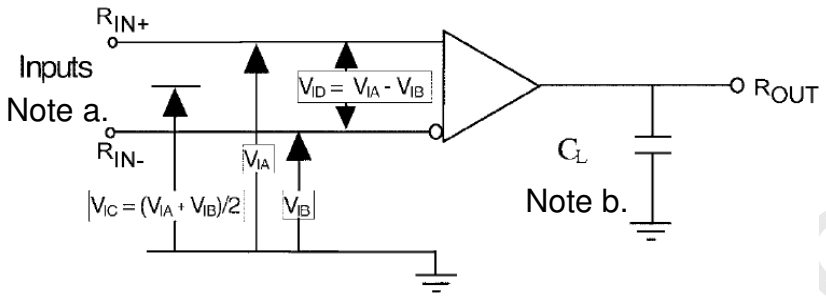
Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V_{DD}	4.5	5.0	5.5	V	(1)
LVDS Input Characteristics	Differential Input Voltage for LVDS Receiver Threshold	High	-	-	+100	mV	(2)
		Low	-100	-	-	mV	
	LVDS skew	t_{SKEW}	-300		300	ps	(3)
	Differential input voltage	$\|V_{ID}\|$	200		600	mV	(4)
	Input voltage range (single-ended)	V_{IN}	0		2.4	V	(4)
	Common mode voltage	V_{CM}	0+ $\|V_{ID}\|/2$	1.2	2.4- $\|V_{ID}\|/2$	V	(4)
Current of Power Supply	(a) Black	I_{DD}	-	1700	-	mA	(5),(6)
	(b) White		-	900	-	mA	
	(c) Dot		-	1900	3000	mA	
Vsync Frequency		f_V	92	120	124	Hz	
Hsync Frequency		f_H	102	134	175	kHz	
Main Frequency		f_{DCLK}	52	70	90	MHz	
Rush Current		I_{RUSH}	-	-	5	A	(7)

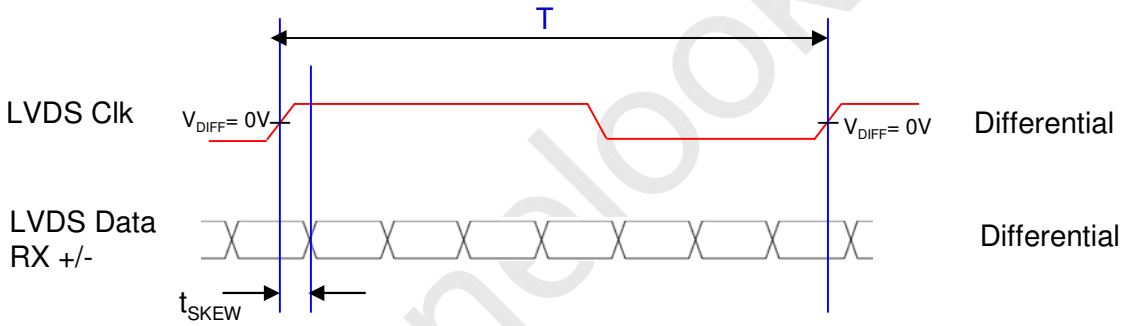
Note (1) The ripple voltage should be controlled under 10% of V_{DD}.

(2) Differential receiver voltage definitions and propagation delay and transition time test circuit

a. All input pulses have frequency = 10MHz, t_R or t_F=1ns
b. C_L includes all probe and fixture capacitance

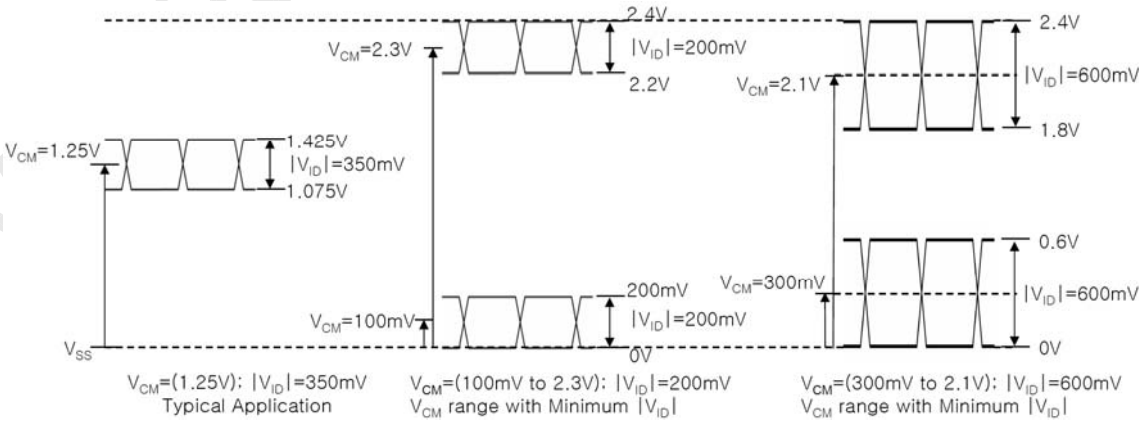


(3) LVDS Receiver DC parameters are measured under static and steady conditions which may not be reflective of its performance in the end application.



where tskew : skew between LVDS clock & LVDS data,
T : 1 period time of LVDS clock
cf) (-/+) of 300psec means LVDS data goes before or after LVDS clock.

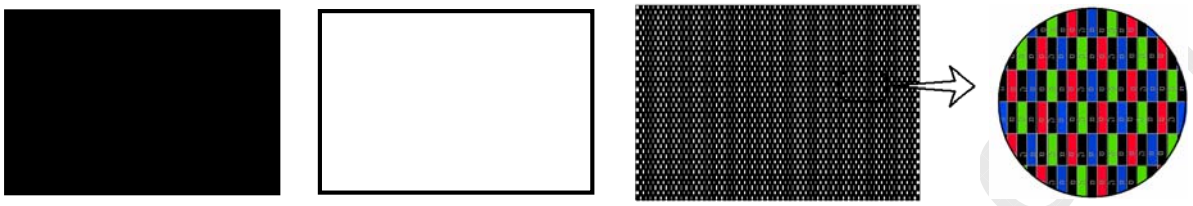
(4) Definition of V_{ID} and V_{CM} using single-end signals



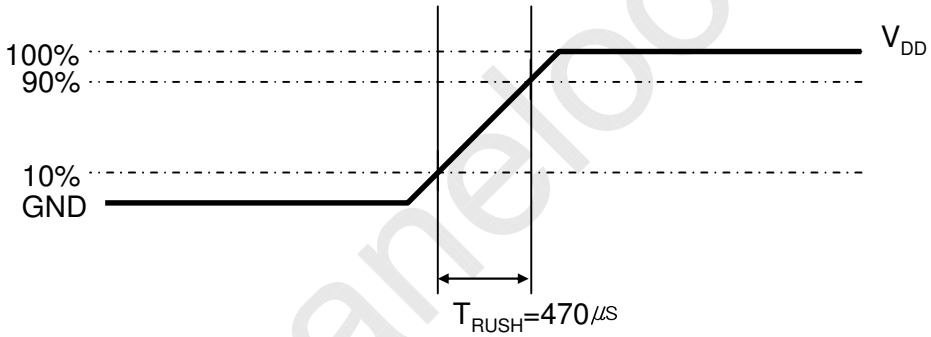
(5) fV=120Hz, fDCLK = 90 MHz, VDD = 5.0V, DC Current.

(6) Power dissipation check pattern (LCD Module only)

a) Black Pattern b) White Pattern c) Dot Pattern



(7) Measurement Condition



Rush Current I_{RUSH} can be measured when T_{RUSH}. is 470μs.

3.2 Back Light Unit

The back light unit is an edge - lighting type with 2 dual CCFTs (Cold Cathode Fluorescent Tube) The characteristics of two dual lamps are shown in the following tables.

Ta=25 ± 2°C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Lamp Current		I_L	4.0	7.5	8.0	mArms	(1)
Lamp Voltage		V_L	-	850	-	Vrms	
Lamp Frequency		f_L	40	-	(80)	kHz	(2)
Operating Life Time		Hr	50,000	-	-	Hour	(3)
Inverter waveform	Asymmetry rate	Wasy	-	-	10	%	(4)
	Distortion rate	Wdis	1.2726	1.414	1.5554		
Startup Voltage		Vs	-	-	0℃ : 1,840 25℃: 1,450	Vrms	(5)

Note (1) Specified values are for a single lamp.
Lamp current is measured with current meter for high frequency as shown below.
Refer to the following block diagram of the back light unit for more information.

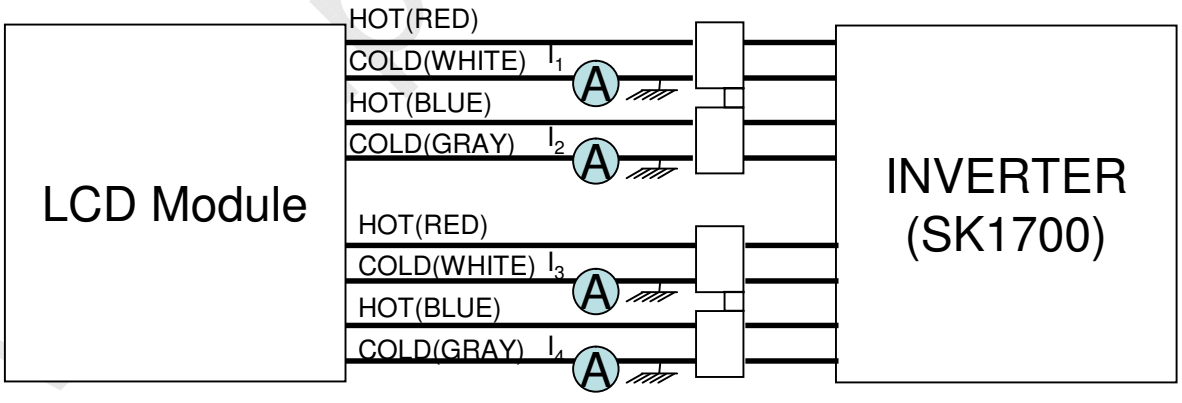


Fig. Measurement point of Lamp Current

(2) Lamp frequency which may produce interference with horizontal synchronous frequency may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

(3) Life time (Hr) is defined as the time when brightness of a lamp unit itself becomes 50% or less than its original value at the condition of Ta = 25±2°C and I_L = 7.5mArms

(4) Designing a system inverter intended to have better display performance, power efficiency and lamp reliability.

They would help increase the lamp lifetime and reduce leakage current.

a. The measurement should be done at typical lamp current.

b. The asymmetry rate of the inverter waveform should be less than 10%.

c. The distortion rate of the waveform should be √2 with ±10% tolerance.

- Inverter output waveform had better be more similar to ideal sine wave.

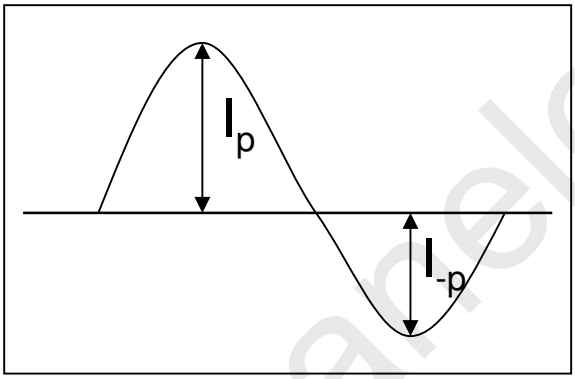


Fig. Wave form of the inverter

- Asymmetry rate

$$\frac{|I_p - I_{-p}|}{I_{rms}} \times 100$$

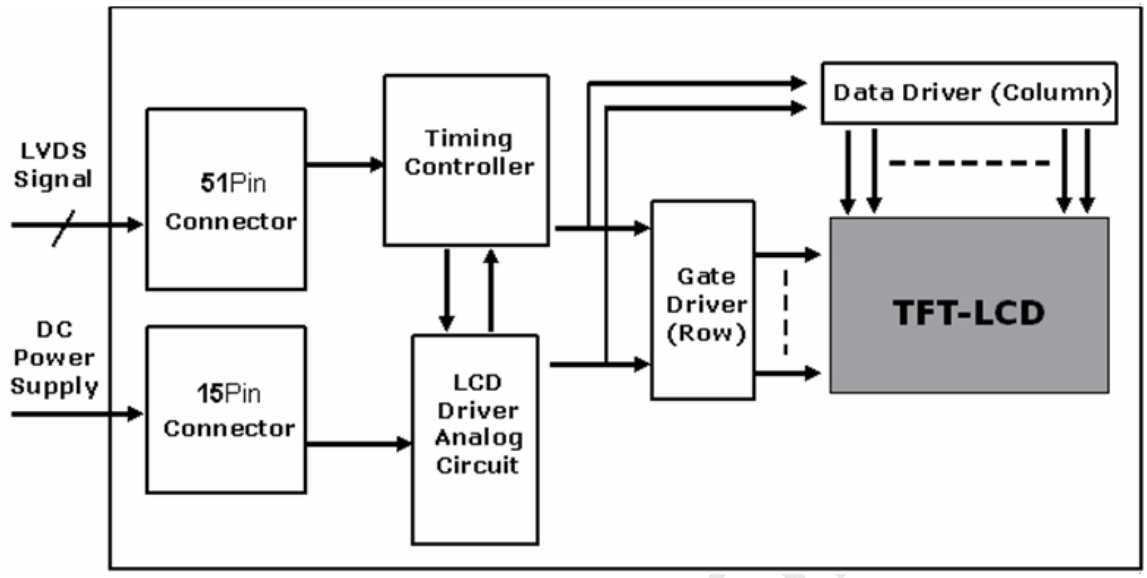
- Distortion rate

$$\left|\frac{I_p}{I_{rms}}\right| \text{ or } \left|\frac{I_{-p}}{I_{rms}}\right|$$

(5) If an inverter has shutdown function, it should keep its output for over 1 second even if the lamp connector is open. Otherwise the lamps may not be turned on.

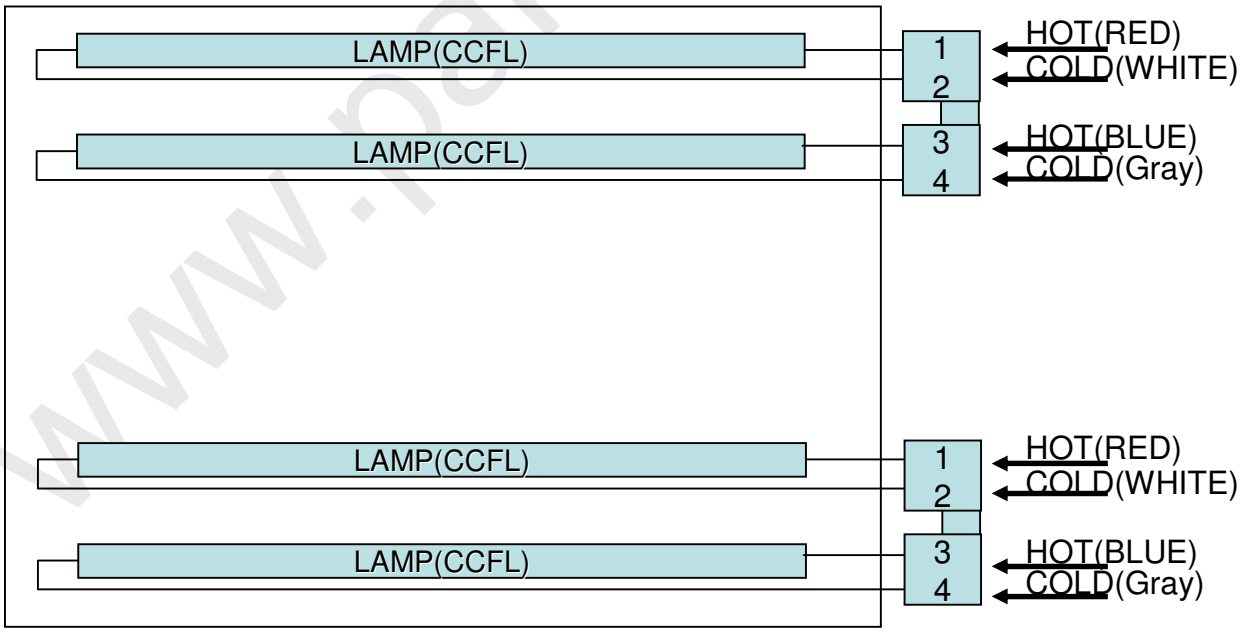
4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 Back Light Unit

Connector : YEON-HO 35001HS-04L



5. Input Terminal Pin Assignment

5.1. Input Signal & Power (Connector : JAE FI-RE51S-HF)

PIN NO	SYMBOL	FUNCTION
1	B_RXO0N	B_Negative Transmission Data of Pixel 0 (ODD data)
2	B_RXO0P	B_Positive Transmission Data of Pixel 0 (ODD data)
3	B_RXO1N	B_Negative Transmission Data of Pixel 1 (ODD data)
4	B_RXO1P	B_Positive Transmission Data of Pixel 1 (ODD data)
5	B_RXO2N	B_Negative Transmission Data of Pixel 2 (ODD data)
6	B_RXO2P	B_Positive Transmission Data of Pixel 2 (ODD data)
7	GND	Power Ground
8	B_RXOCN	B_Negative Sampling Clock (ODD data)
9	B_RXOCP	B_Positive Sampling Clock (ODD data)
10	GND	Power Ground
11	B_RXO3N	B_Negative Transmission Data of Pixel 3 (ODD data)
12	B_RXO3P	B_Positive Transmission Data of Pixel 3 (ODD data)
13	GND	Power Ground
14	B_RXE0N	B_Negative Transmission Data of Pixel 0 (EVEN data)
15	B_RXE0P	B_Positive Transmission Data of Pixel 0 (EVEN data)
16	B_RXE1N	B_Negative Transmission Data of Pixel 1 (EVEN data)
17	B_RXE1P	B_Positive Transmission Data of Pixel 1 (EVEN data)
18	B_RXE2N	B_Negative Transmission Data of Pixel 2 (EVEN data)
19	B_RXE2P	B_Positive Transmission Data of Pixel 2 (EVEN data)
20	GND	Power Ground
21	B_RXECN	B_Negative Sampling Clock (EVEN data)
22	B_RXECP	B_Positive Sampling Clock (EVEN data)
23	GND	Power Ground
24	B_RXE3N	B_Negative Transmission Data of Pixel 3 (EVEN data)
25	B_RXE3P	B_Positive Transmission Data of Pixel 3 (EVEN data)
26	GND	Power Ground
27~51	Continue to the next page	

PIN NO	SYMBOL	FUNCTION
27	F_RXO0N	F_Negative Transmission Data of Pixel 0 (ODD data)
28	F_RXO0P	F_Positive Transmission Data of Pixel 0 (ODD data)
29	F_RXO1N	F_Negative Transmission Data of Pixel 1 (ODD data)
30	F_RXO1P	F_Positive Transmission Data of Pixel 1 (ODD data)
31	F_RXO2N	F_Negative Transmission Data of Pixel 2 (ODD data)
32	F_RXO2P	F_Positive Transmission Data of Pixel 2 (ODD data)
33	GND	Power Ground
34	F_RXOCN	F_Negative Sampling Clock (ODD data)
35	F_RXOCP	F_Positive Sampling Clock (ODD data)
36	GND	Power Ground
37	F_RXO3N	F_Negative Transmission Data of Pixel 3 (ODD data)
38	F_RXO3P	F_Positive Transmission Data of Pixel 3 (ODD data)
39	GND	Power Ground
40	F_RXE0N	F_Negative Transmission Data of Pixel 0 (EVEN data)
41	F_RXE0P	F_Positive Transmission Data of Pixel 0 (EVEN data)
42	F_RXE1N	F_Negative Transmission Data of Pixel 1 (EVEN data)
43	F_RXE1P	F_Positive Transmission Data of Pixel 1 (EVEN data)
44	F_RXE2N	F_Negative Transmission Data of Pixel 2 (EVEN data)
45	F_RXE2P	F_Positive Transmission Data of Pixel 2 (EVEN data)
46	GND	Power Ground
47	F_RXECN	F_Negative Sampling Clock (EVEN data)
48	F_RXECP	F_Positive Sampling Clock (EVEN data)
49	GND	Power Ground
50	F_RXE3N	F_Negative Transmission Data of Pixel 3 (EVEN data)
51	F_RXE3P	F_Positive Transmission Data of Pixel 3 (EVEN data)

Note) Pin number starts from Left side

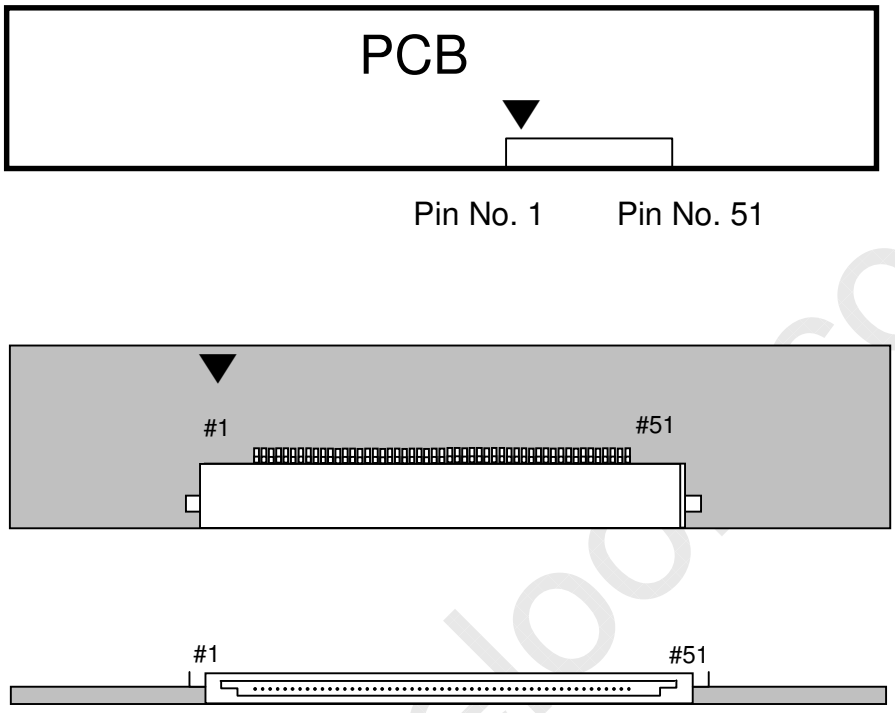
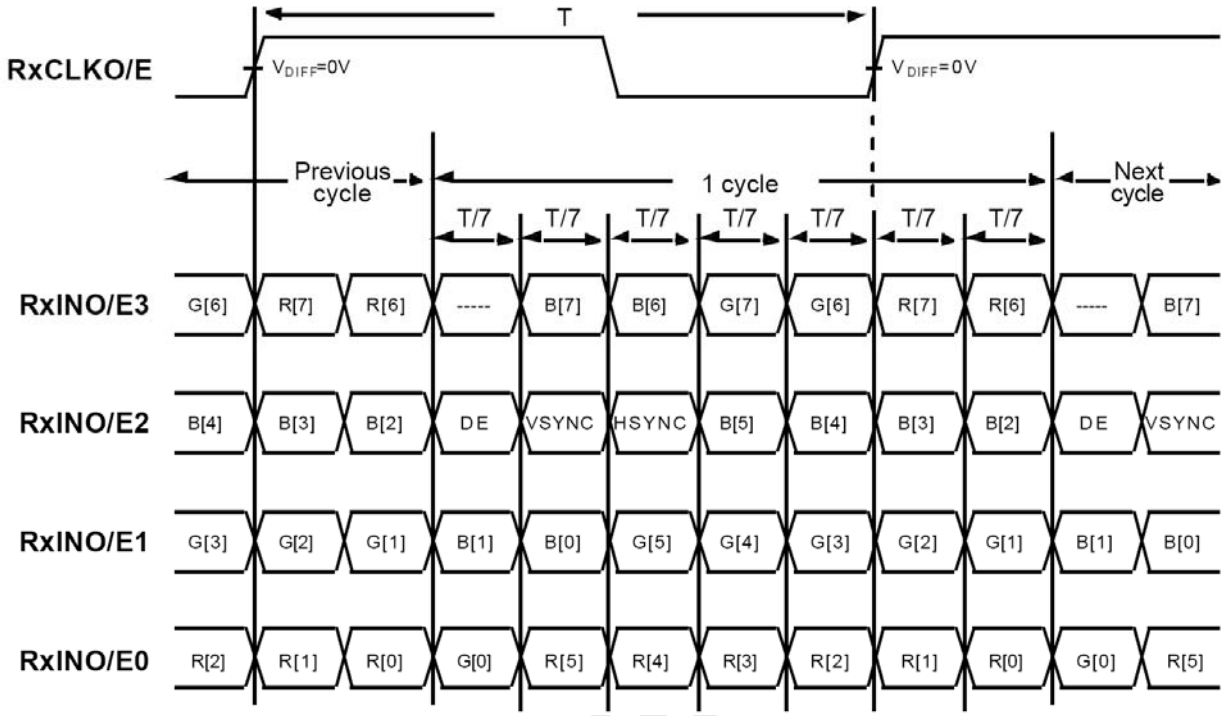


Fig. Connector diagram

a. All GND pins should be connected together and also be connected to the LCD's metal chassis.
b. All power input pins should be connected together.
c. All NC pins should be separated from other signal or power.

5.1.1 Timing Diagrams of LVDS For Transmitting

LVDS Receiver : Integrated T-CON



5.1.2. Input Signal & Power (Connector : YEONHO, 12505WR-15)

<table>
<tr><th>PIN NO</th><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>OD_EN</td><td>Enable Over Drive Function Input pin
<table><tr><th>OD EN Pin</th><th>OD Function</th></tr><tr><td>0 (GND)</td><td>Disable</td></tr><tr><td>1 (+3.3V)</td><td>Enable</td></tr></table></td></tr>
<tr><td>2</td><td>NC</td><td>NC</td></tr>
<tr><td>3</td><td>NC</td><td>NC</td></tr>
<tr><td>4</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>5</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>6</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>7</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>8</td><td>NC</td><td>* CE (For LCD internal use only. Do not Connect)</td></tr>
<tr><td>9</td><td>NC</td><td>* CTL(For LCD internal use only. Do not connect)</td></tr>
<tr><td>10</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>11</td><td>VDD</td><td>Power Supply : +5V</td></tr>
<tr><td>12</td><td>VDD</td><td>Power Supply : +5V</td></tr>
<tr><td>13</td><td>VDD</td><td>Power Supply : +5V</td></tr>
<tr><td>14</td><td>VDD</td><td>Power Supply : +5V</td></tr>
<tr><td>15</td><td>VDD</td><td>Power Supply : +5V</td></tr>
</table>

5.2 LVDS Interface (1)

5.2.1 Front _ Odd Pixel Data

LVDS Transmitter (THC63LVD103) Signal Interface						
Input pin		Input signal		Output signal	LTM230HU01 interface	
No	symbol	symbol	Function		Terminal	Symbol
59	TD0	F_RO2	Red Odd Pixel Data(LSB)	TD- / TD+	37 / 38	F_RXO3N / F_RXO3P
61	TD1	F_RO3	Red Odd Pixel Data			
33	TA0	F_RO4	Red Odd Pixel Data	TA- / TA+	27 / 28	F_RXO0N / F_RXO0P
34	TA1	F_RO5	Red Odd Pixel Data			
35	TA2	F_RO6	Red Odd Pixel Data			
36	TA3	F_RO7	Red Odd Pixel Data			
37	TA4	F_RO8	Red Odd Pixel Data			
38	TA5	F_RO9	Red Odd Pixel Data(MSB)			
62	TD2	F_GO2	Green Odd Pixel Data(LSB)	TD- / TD+	37 / 38	F_RXO3N / F_RXO3P
63	TD3	F_GO3	Green Odd Pixel Data			
40	TA6	F_GO4	Green Odd Pixel Data	TA- / TA+	27 / 28	F_RXO0N / F_RXO0P
41	TB0	F_GO5	Green Odd Pixel Data	TB- / TB+	29 / 30	F_RXO1N / F_RXO1P
42	TB1	F_GO6	Green Odd Pixel Data			
44	TB2	F_GO7	Green Odd Pixel Data			
45	TB3	F_GO8	Green Odd Pixel Data			
46	TB4	F_GO9	Green Odd Pixel Data(MSB)			
64	TD4	F_BO2	Blue Odd Pixel Data(LSB)	TD- / TD+	37 / 38	F_RXO3N / F_RXO3P
1	TD5	F_BO3	Blue Odd Pixel Data			
48	TB5	F_BO4	Blue Odd Pixel Data	TB- / TB+	29 / 30	F_RXO1N / F_RXO1P
49	TB6	F_BO5	Blue Odd Pixel Data			
50	TC0	F_BO6	Blue Odd Pixel Data	TC- / TC+	31 / 32	F_RXO2N / F_RXO2P
52	TC1	F_BO7	Blue Odd Pixel Data			
53	TC2	F_BO8	Blue Odd Pixel Data			
54	TC3	F_BO9	Blue Odd Pixel Data(MSB)			

5.2 LVDS Interface (1)

5.2.2 Front _ Even Pixel Data

LVDS Transmitter (THC63LVD103) Signal Interface						
Input pin		Input signal		Output signal	LTM230HU01 interface	
No	symbol	symbol	Function		Terminal	Symbol
59	TD0	F_RE2	Red Even Pixel Data(LSB)	TD- / TD+	50 / 51	F_RXE3N / F_RXE3P
61	TD1	F_RE3	Red Even Pixel Data			
33	TA0	F_RE4	Red Even Pixel Data	TA- / TA+	40 / 41	F_RXE0N / F_RXE0P
34	TA1	F_RE5	Red Even Pixel Data			
35	TA2	F_RE6	Red Even Pixel Data			
36	TA3	F_RE7	Red Even Pixel Data			
37	TA4	F_RE8	Red Even Pixel Data			
38	TA5	F_RE9	Red Even Pixel Data(MSB)			
62	TD2	F_GE2	Green Even Pixel Data(LSB)	TD- / TD+	50 / 51	F_RXE3N / F_RXE3P
63	TD3	F_GE3	Green Even Pixel Data			
40	TA6	F_GE4	Green Even Pixel Data	TA- / TA+	40 / 41	F_RXE0N / F_RXE0P
41	TB0	F_GE5	Green Even Pixel Data	TB- / TB+	42 / 43	F_RXE1N / F_RXE1P
42	TB1	F_GE6	Green Even Pixel Data			
44	TB2	F_GE7	Green Even Pixel Data			
45	TB3	F_GE8	Green Even Pixel Data			
46	TB4	F_GE9	Green Even Pixel Data(MSB)			
64	TD4	F_BE2	Blue Even Pixel Data(LSB)	TD- / TD+	50 / 51	F_RXE3N / F_RXE3P
1	TD5	F_BE3	Blue Even Pixel Data			
48	TB5	F_BE4	Blue Even Pixel Data	TB- / TB+	42 / 43	F_RXE1N / F_RXE1P
49	TB6	F_BE5	Blue Even Pixel Data			
50	TC0	F_BE6	Blue Even Pixel Data	TC- / TC+	44 / 45	F_RXE2N / F_RXE2P
52	TC1	F_BE7	Blue Even Pixel Data			
53	TC2	F_BE8	Blue Even Pixel Data			
54	TC3	F_BE9	Blue Even Pixel Data(MSB)			

5.3 LVDS Interface (2)

5.3.1 Back _ Odd Pixel Data

LVDS Transmitter (THC63LVD103) Signal Interface						
Input pin		Input signal		Output signal	LTM230HU01 interface	
No	symbol	symbol	Function		Terminal	Symbol
59	TD0	B_RO2	Red Odd Pixel Data(LSB)	TD- / TD+		B_RXO3N / B_RXO3P
61	TD1	B_RO3	Red Odd Pixel Data			
33	TA0	B_RO4	Red Odd Pixel Data	TA- / TA+	1 / 2	B_RXO0N / B_RXO0P
34	TA1	B_RO5	Red Odd Pixel Data			
35	TA2	B_RO6	Red Odd Pixel Data			
36	TA3	B_RO7	Red Odd Pixel Data			
37	TA4	B_RO8	Red Odd Pixel Data			
38	TA5	B_RO9	Red Odd Pixel Data(MSB)			
62	TD2	B_GO2	Green Odd Pixel Data(LSB)	TD- / TD+	11 / 12	B_RXO3N / B_RXO3P
63	TD3	B_GO3	Green Odd Pixel Data			
40	TA6	B_GO4	Green Odd Pixel Data	TA- / TA+	1 / 2	B_RXO0N / B_RXO0P
41	TB0	B_GO5	Green Odd Pixel Data	TB- / TB+	3 / 4	B_RXO1N / B_RXO1P
42	TB1	B_GO6	Green Odd Pixel Data			
44	TB2	B_GO7	Green Odd Pixel Data			
45	TB3	B_GO8	Green Odd Pixel Data			
46	TB4	B_GO9	Green Odd Pixel Data(MSB)			
64	TD4	B_BO2	Blue Odd Pixel Data(LSB)	TD- / TD+	11 / 12	B_RXO3N / B_RXO3P
1	TD5	B_BO3	Blue Odd Pixel Data			
48	TB5	B_BO4	Blue Odd Pixel Data	TB- / TB+	3 / 4	B_RXO1N / B_RXO1P
49	TB6	B_BO5	Blue Odd Pixel Data			
50	TC0	B_BO6	Blue Odd Pixel Data	TC- / TC+	5 / 6	B_RXO2N / B_RXO2P
52	TC1	B_BO7	Blue Odd Pixel Data			
53	TC2	B_BO8	Blue Odd Pixel Data			
54	TC3	B_BO9	Blue Odd Pixel Data(MSB)			

5.3 LVDS Interface (2)

5.3.2 Back _ Even Pixel Data

LVDS Transmitter (THC63LVD103) Signal Interface						
Input pin		Input signal		Output signal	LTM230HU01 interface	
No	symbol	symbol	Function		Terminal	Symbol
59	TD0	RE2	Red Even Pixel Data(LSB)	TD- / TD+		B_RXE3N / B_RXE3P
61	TD1	B_RE3	Red Even Pixel Data			
33	TA0	B_RE4	Red Even Pixel Data	TA- / TA+	14 / 15	B_RXE0N / B_RXE0P
34	TA1	B_RE5	Red Even Pixel Data			
35	TA2	B_RE6	Red Even Pixel Data			
36	TA3	B_RE7	Red Even Pixel Data			
37	TA4	B_RE8	Red Even Pixel Data			
38	TA5	B_RE9	Red Even Pixel Data(MSB)			
62	TD2	B_GE2	Green Even Pixel Data(LSB)	TD- / TD+	24 / 25	B_RXE3N / B_RXE3P
63	TD3	B_GE3	Green Even Pixel Data			
40	TA6	B_GE4	Green Even Pixel Data	TA- / TA+	14 / 15	B_RXE0N / B_RXE0P
41	TB0	B_GE5	Green Even Pixel Data	TB- / TB+	16 / 17	B_RXE1N / B_RXE1P
42	TB1	B_GE6	Green Even Pixel Data			
44	TB2	B_GE7	Green Even Pixel Data			
45	TB3	B_GE8	Green Even Pixel Data			
46	TB4	B_GE9	Green Even Pixel Data(MSB)			
64	TD4	B_BE2	Blue Even Pixel Data(LSB)	TD- / TD+	24 / 25	B_RXE3N / B_RXE3P
1	TD5	B_BE3	Blue Even Pixel Data			
48	TB5	B_BE4	Blue Even Pixel Data	TB- / TB+	16 / 17	B_RXE1N / B_RXE1P
49	TB6	B_BE5	Blue Even Pixel Data			
50	TC0	B_BE6	Blue Even Pixel Data	TC- / TC+	18 / 19	B_RXE2N / B_RXE2P
52	TC1	B_BE7	Blue Even Pixel Data			
53	TC2	B_BE8	Blue Even Pixel Data			
54	TC3	B_BE9	Blue Even Pixel Data(MSB)			

5.4 Back Light Unit

	Pin No.	Input	Color	Function
Upper	1	Hot1	RED	High Voltage
	2	Cold1	White	Ground
	3	Hot2	Blue	High Voltage
	4	Cold2	Gray	Ground
Lower	1	Hot1	RED	High Voltage
	2	Cold1	White	Ground
	3	Hot2	Blue	High Voltage
	4	Cold2	Gray	Ground
	Connector Part No.	YEON-HO 35001HS-04SL		

5.5 Input Signals, Basic Display Colors and Gray Scale of Each Color

COLOR	DISPLAY (8bit)	DATA SIGNAL																								GRAY SCALE LEVEL
		RED								GREEN								BLUE								
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			R3~ R252
	↓ LIGHT	:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R253
		0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R254
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R255
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			G3~ G252
	↓ LIGHT	:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G253
		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G254
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G255
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	B2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			B3~ B252
	↓ LIGHT	:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	B253
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	B254
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	B255

Note (1) Definition of Gray :
Rn : Red Gray, Gn : Green Gray, Bn : Blue Gray (n = Gray level)
Input Signal : 0 = Low level voltage, 1 = High level voltage

6. Interface Timing

6.1 Timing Parameters (DE only mode)

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	Unit	NOTE
Clock	Frequency	$1/T_C$	52	70	90	MHz	-
Hsync		F_H	102	134	175	kHz	-
Vsync		F_V	92	120	124	Hz	-
Vertical Display Term	Active Display Period	T_{VD}	1080	1080	1080	Lines	-
	Vertical Total	T_V	1110	1120	1744	Lines	-
Horizontal Display Term	Active Display Period	T_{HD}	1920	1920	1920	Clocks	Pixel /clock
	Horizontal Total	T_H	2056	2080	2224	clocks	Pixel /clock

Note (1) This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

(2) Test Point : TTL control signal and CLK at LVDS Tx input terminal in system

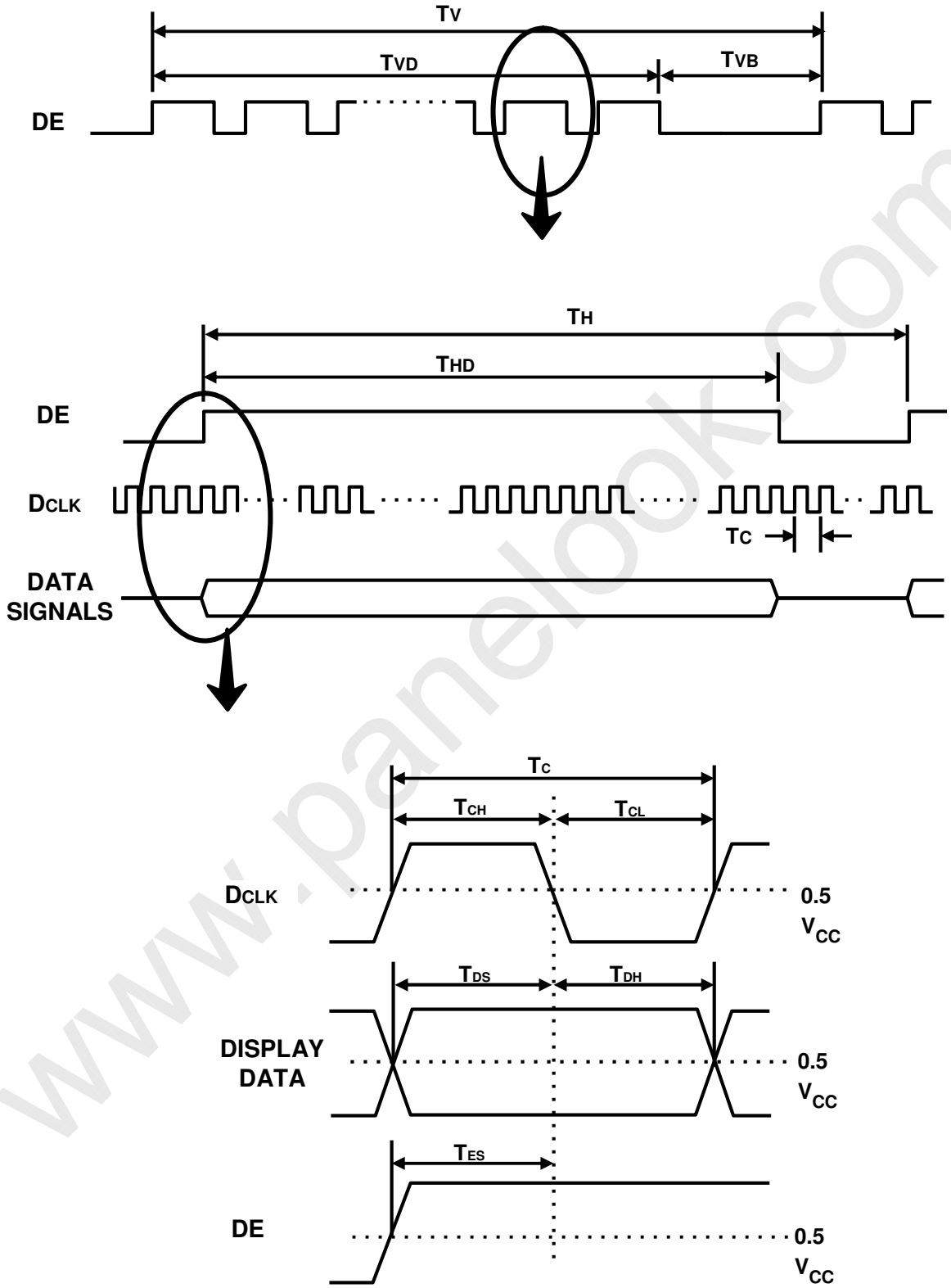
(3) Internal Vcc = 3.3V

(4) Best operation clock frequency is 70 MHz (120Hz)

(5) Clock frequency = Frame frequency x T_V(Typ) x T_H(Typ)

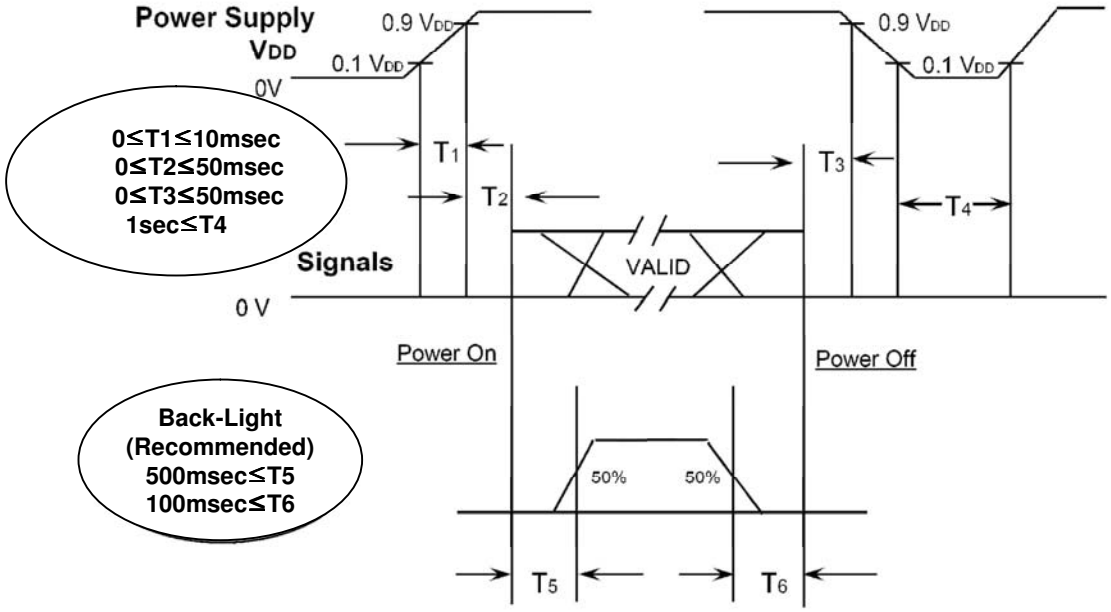
(6) Max, Min variation range is at main clock Typ value

6.2 Timing diagrams of interface signal (DE only mode)



6.3 Power ON/OFF Sequence

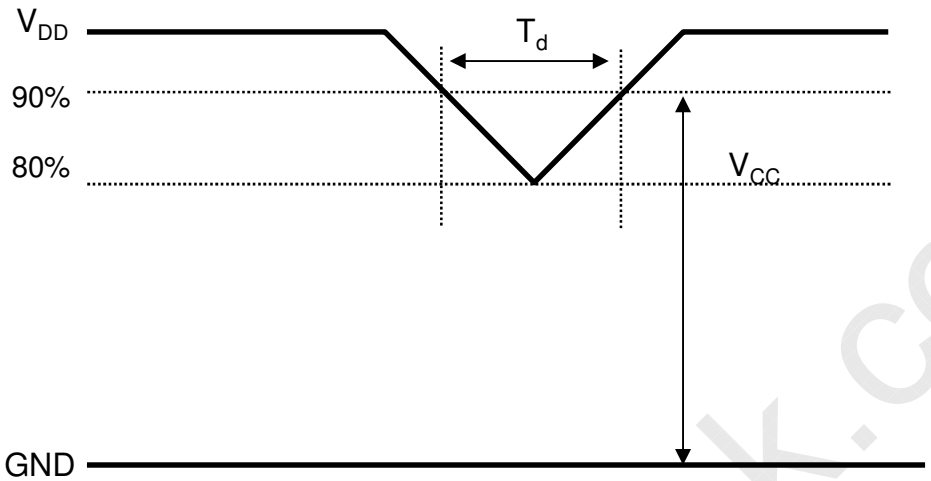
To prevent a latch-up or DC operation of the LCD Module, the power on/off sequence should be as the diagram below.



T1 : V_{DD} rising time from 10% to 90%
T2 : The time from V_{DD} to valid data at power ON.
T3 : The time from valid data off to V_{DD} off at power Off.
T4 : V_{DD} off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

- The supply voltage of the external system for the Module input should be the same as the definition of V_{DD}.
- Apply the lamp voltage within the LCD operation range. When the back light turns on before the LCD operation or the LCD turns off before the back light turns off, the display may momentarily show abnormal screen.
- In case of V_{DD} = off level, please keep the level of input signals low or keep a high impedance.
- T4 should be measured after the Module has been fully discharged between power off and on period.
- Interface signal should not be kept at high impedance when the power is on.

6.4 VDD Power Dip Condition



$4.5V \leq V_{DD} \leq 5.5V$
If V_{DD}(typ.) x 80% $\leq V_{CC} \leq V_{DD}$(typ) x 90%
Then, 0<Td ≤20msec

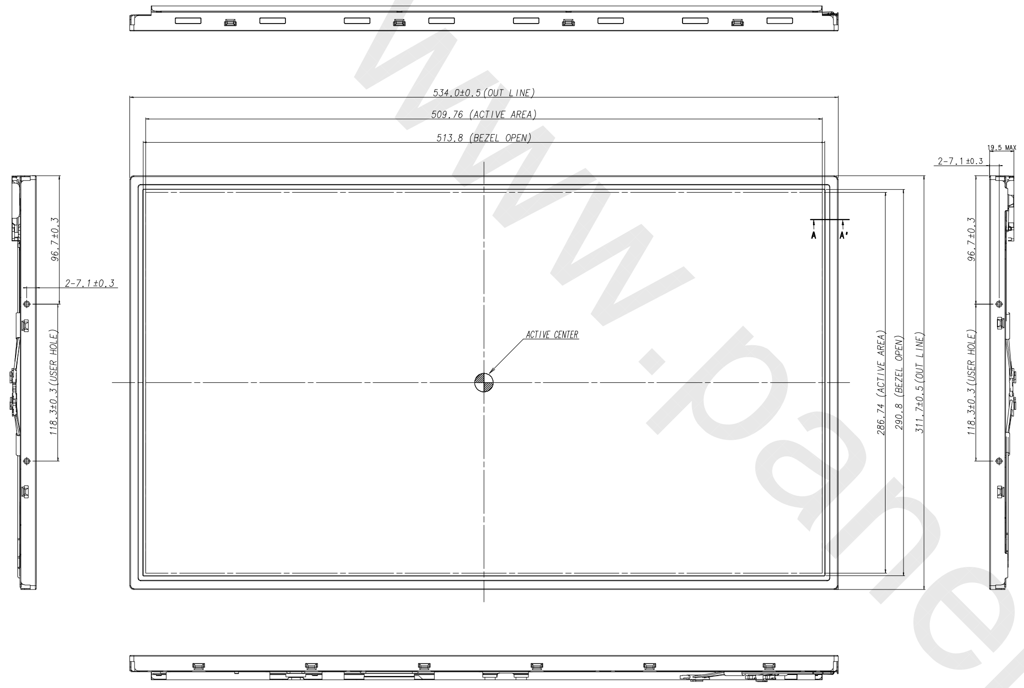
Note (1) The above conditions are for the glitch of the input voltage.
(2) For stable operation of an LCD Module power, please follow them.
i.e., if typ VDD x 80% $\leq$ Vcc $\leq$ typ VDD x 90%, then T_d should be less than 20ms.

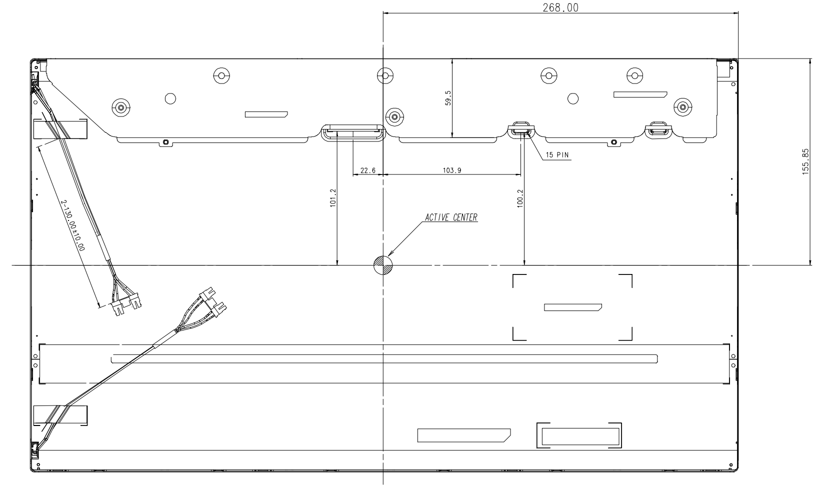
PRODUCT INFORMATION

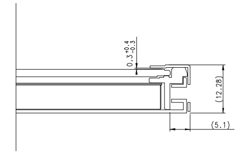
7. Outline Dimension

[Refer to the next page]

NO	PART NAME	CODE NO	SPECIFICATION	Q'TY	WEIGHT FINISH	MATERIAL	UNFOLDED DIM. OF MATERIAL	REMARK
01		-	OUTLINE	1				







SECTION A-A' (2:1)

NOTES
1. BACKLIGHT : 4 COLD CATHODE FLUORESCENT LAMPS
2. I/F CONNECTOR SPEC.
- MAKER: JAE
- PART NO.: FI-RE51S-HF
3. LAMP CONNECTOR SPEC.
- MAKER: YEON HO
- PART NO.: 35001HS-04L OR EQUIVALENT
4. USER MOUNTING TORQUE SPEC : 4 ~ 6 kgf-cm

5. BLACK MATRIX SPEC (When set up at standing)

- |A - B| ≤ 2.0 mm
- |C - D| ≤ 2.0 mm

BLACK MATRIX

GENERAL TOLERANCE			
STEP	LEVEL 1	LEVEL 2	LEVEL 3
0 < X ≤ 4	±0.05	±0.1	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.4	±0.8

REV | DATE | DESCRIPTION OF REVISION | REASON | CHK'D BY
UNIT: mm | SCALE: / | TOLERANCE
DRA'N BY: J.K. KIM 09.11.03 | DES'D BY | CHK'D BY | APP'D BY
MODEL NAME | PART/SHEET NAME | SPEC. NO | CODE NO.
SAMSUNG ELECTRONICS

8. General Precautions

8.1 Handling

(a) When the module is assembled, it should be attached to the system firmly using all mounting holes. Be careful not to twist and bend the module.

(b) Because the inverter uses high voltages, it should be disconnected from power source before it is assembled or disassembled.

(c) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, it may cause improper operation or damage to the module and CCFT back light.

(d) Note that polarizer films are very fragile and could be damaged easily. Do not press or scratch the surface harder than a HB pencil lead.

(e) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining or discoloration may occur.

(f) If the surface of the polarizer is dirty, clean it using absorbent cotton or soft cloth.

(g) Desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might cause permanent damage to the polarizer due to chemical reaction.

(h) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away with soap thoroughly.

(i) Protect the Module from static, or the CMOS Gate Array IC would be damaged.

(j) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(k) Do not disassemble the Module.

(l) Do not pull or fold the lamp wire.

(m) Do not adjust the variable resistor located on the Module.

(n) Protection film for polarizer on the Module should be slowly peeled off just before use so that the electrostatic charge can be minimized.

(o) Pins of I/F connector should not be touched directly with bare hands.

8.2 Storage

(a) Do not leave the Module in high temperature, and high humidity for a long time. It is highly recommended to store the Module with temperature from 0 to 35℃ and relative humidity of less than 70%.

(b) Do not store the TFT-LCD Module in direct sunlight.

(c) The Module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storing.

8.3 Operation

(a) Do not connect or disconnect the Module in the "Power On" condition.

(b) Power supply should always be turned on/off by the item 6.3 "Power on/off sequence"

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The cable between the back light connector and its inverter power supply should be connected directly with a minimized length. A longer cable between the back light and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

8.4 Operation Condition Guide

(a) The LCD product should be operated under normal conditions.
Normal condition is defined as below;
- Temperature : 20±15℃
- Humidity : 65±20%
- Display pattern : continually changing pattern (Not stationary)

(b) If the product will be used in extreme conditions such as high temperature, humidity, display patterns or operation time etc.., It is strongly recommended to contact SEC for Application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at Airports, Transit Stations, Banks, Stock market, and Controlling systems.

8.5 Others

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on)
Otherwise the Module may be damaged.

(d) If the Module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.
To avoid image sticking, it is recommended to use a screen saver.

(e) This Module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

(f) Please contact SEC in advance when you display the same pattern for a long time.